UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/624,776 | 07/22/2003 | Karsten Wieczorek | 2000.104300 | 6782 |

23720 7590 02/04/2005

WILLIAMS, MORGAN & AMERSON, P.C.
10333 RICHMOND, SUITE 1100
HOUSTON, TX 77042

| EXAMINER | |
|---|---|
| NGUYEN, THANH T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2813 | |

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/624,776 | WIECZOREK ET AL. | |
| | Examiner | Art Unit | |
| | Thanh T. Nguyen | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sh t with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9 and 22-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 22-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119 (a)-(d).

### *Information Disclosure Statement*

The information disclosure statement filed 1/23/04 has been considered.

### *Oath/Declaration*

Oath/Declaration filed on 7/22/03 has been considered.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 6-7 recite the limitation "said layer of material" in line 1. There is insufficient antecedent basis for this limitation in the claim. It is suggested to change to "said second layer of material".

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7-8, 22-23, 26-28, 30-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishida et al. (U.S. Patent No. 6,344,396).

Referring to figures 1a-1j, Ishida et al. teaches in claim 1, A method of forming a semiconductor device feature, the method comprising:

providing a substrate (10) having a first layer (12) formed thereon;

covering said substrate with a second layer of material (14);

implanting ions (15a/15b) into said second layer of material (14') to modify a structure of the material of said second layer (see figure 1D);

patterning said second layer of material (14) and said first layer by photolithography to form said semiconductor device feature in said first layer (see figure 1c); and

removing said patterned second layer of material, whereby a selectivity in removing

said patterned second layer is increased by the implanting of said ions (see figure 1e-1f, col. 11, lines 31-67, col. 12, lines 1-65), wherein the layer 14' has been removed). It is inherent that the implanted region would have a higher etch selectivity.

2. The method of claim 1, wherein said ions are substantially inert ions (see col. 11, lines 51-67).

3. The method of claim 1, wherein said ions are at least one of argon ions, xenon ions, germanium ions and silicon ions (see col. 11, lines 51-67).

4. The method of claim 1, wherein the ion dose is in the range of approximately 1x1013 to 5x 1015 ions/cm2 (see col. 12, lines 30-40).

5. The method of claim 1, wherein the ion energy is in the range of approximately 5-80 kev (see col. 12, lines 30-40)..

7. The method of claim 1, wherein said layer of material is comprised of an inorganic material (14, nitride is an inorganic material).

8. The method of claim 1, wherein the material of said layer of material is one of silicon nitride and silicon reacted nitride (dielectric nitride is short for silicon nitride known in semiconductor).

22. A method, comprising:

providing a substrate (10) having a first layer of material formed thereabove;

depositing a second layer of material (14) above said first layer of material; and

implanting ions(15a/15b) into said second layer of material (14') to modify a structure of the material of said second layer of material and thereby increase an etch selectivity of said second layer of material relative to said first layer of material (see figure 1e-1f, col. 11, lines 31-67, col. 12, lines 1-65), wherein the layer 14' has been removed). It is inherent that the implanted region would have a higher etch selectivity.

23. The method of claim 22, wherein said first layer of material comprises a gate electrode material (12, see col. 10, lines 33-34).

26. The method of claim 22, wherein said ions comprise at least one of argon ions, xenon ions, germanium ions and silicon ions (see col. 11, lines 51-67).

27. The method of claim 22, wherein said ions are substantially inert ions (see col. 11, lines 51-67).

28. The method of claim 22, wherein an implant energy of an ion implant process performed to implant said ions is selected such that the structure of the material comprising the second layer of material is modified substantially throughout an entire thickness of said second layer of material (see figure 1e-1f).

30. The method of claim 22, further comprising performing at least one etch process to define a feature in said first layer of material (see figures 1a).

31. The method of claim30, further comprising performing an etching process to remove a portion of said second layer of material above said feature in said first layer of material (see figures 1b-1c, cols. 11, lines 7-30).

Claims 1-3, 7, 22-23, 25-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Long et al. (U.S. Patent No. 6,153,534).

Referring to figures 1-10b, Long et al. teaches in claim 1, A method of forming a semiconductor device feature, the method comprising:

providing a substrate (204) having a first layer (212) formed thereon;

covering said substrate with a second layer of material (250);

implanting ions (see figure 6a-6b) into said second layer of material (250) to modify a structure of the material of said second layer (see figure 1D);

patterning said second layer of material (250) and said first layer by photolithography to form said semiconductor device feature in said first layer (see figure 7); and

removing said patterned second layer of material, whereby a selectivity in removing said patterned second layer is increased by the implanting of said ions (see figure 9a-9b, col. 6, lines 54-67, col. 7, lines 1-18), wherein the layer 250 has been removed). It is inherent that the implanted region would have a higher etch selectivity, see col. 5, lines 44-65).

2. The method of claim 1, wherein said ions are substantially inert ions (see col. 5, lines 44-57).

3. The method of claim 1, wherein said ions are at least one of argon ions, xenon ions, germanium ions and silicon ions (see col. 5, lines 44-57).

7. The method of claim 1, wherein said layer of material is comprised of an inorganic material (250, oxide is an inorganic material).

22. A method, comprising:

providing a substrate (204) having a first layer of material (212) formed thereabove;

depositing a second layer of material (250) above said first layer of material; and implanting ions(see figure 6a-6b) into said second layer of material (250) to modify a structure of the material of said second layer of material and thereby increase an etch selectivity of said second layer of material relative to said first layer of material (see figure 9a-9b, col. 6, lines 54-67, col. 7, lines 1-18), wherein the layer 250 has been removed). It is inherent that the implanted region would have a higher etch selectivity, see col. 5, lines 44-65).

23. The method of claim 22, wherein said first layer of material comprises a

gate electrode material (212, see col. 4, lines 29-34).

25. The method of claim 22, wherein said first layer of material comprises a gate electrode material and said second layer of material comprises an anti-reflective coating material.

26. The method of claim 22, wherein said ions comprise at least one of argon ions, xenon ions, germanium ions and silicon ions (see col. 5, lines 44-57).

27. The method of claim 22, wherein said ions are substantially inert ions (see col. 5, lines 44-57).

28. The method of claim 22, wherein an implant energy of an ion implant process performed to implant said ions is selected such that the structure of the material comprising the second layer of material is modified substantially throughout an entire thickness of said second layer of material (see figure 6a-6b).

Regarding to claim 29, wherein an implant energy of an ion implant process performed to implant said ions is selected such that said implanted ions are substantially located adjacent an interface between said first layer of material and said second layer of material (see figures 6a-6b).

30. The method of claim 22, further comprising performing at least one etch process to define a feature in said first layer of material (see figures 4a-4b).

31. The method of claim 30, further comprising performing an etching process to remove a portion of said second layer of material above said feature in said first layer of material (see figures 6-8).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 24-25, 32-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida et al. (U.S. Patent No. 6,344,396) as applied to claims 1-5, 7-8, 22-23, 26-28, 30-31 or Long et al. (U.S. Patent No. 6,153,534) as applied to claims 1-3, 7, 22-23, 25-31 in view of Iyer et al. (U.S. Patent No. 6,121,133).

Referring to figures 1a-1j, Ishida et al. teaches in claim 1, A method of forming a semiconductor device feature, the method comprising:

providing a substrate (10) having a first layer (12) formed thereon;

covering said substrate with a second layer of material (14);

implanting ions (15a/15b) into said second layer of material (14') to modify a structure of the material of said second layer (see figure 1D);

patterning said second layer of material (14) and said first layer by photolithography to form said semiconductor device feature in said first layer (see figure 1c); and

removing said patterned second layer of material, whereby a selectivity in removing said patterned second layer is increased by the implanting of said ions (see figure 1e-1f, col. 11, lines 31-67, col. 12, lines 1-65), wherein the layer 14' has been removed). It is inherent that the implanted region would have a higher etch selectivity.

2. The method of claim 1, wherein said ions are substantially inert ions (see col. 11, lines 51-67).

3. The method of claim 1, wherein said ions are at least one of argon ions, xenon ions, germanium ions and silicon ions (see col. 11, lines 51-67).

4. The method of claim 1, wherein the ion dose is in the range of approximately 1x1013 to 5x 1015 ions/cm2 (see col. 12, lines 30-40).

5. The method of claim 1, wherein the ion energy is in the range of approximately 5-80 kev (see col. 12, lines 30-40)..

7. The method of claim 1, wherein said layer of material is comprised of an inorganic material (14, nitride is an inorganic material).

8. The method of claim 1, wherein the material of said layer of material is one of silicon nitride and silicon reacted nitride (dielectric nitride is short for silicon nitride known in semiconductor).

22. A method, comprising:

providing a substrate (10) having a first layer of material formed thereabove;

depositing a second layer of material (14) above said first layer of material; and

implanting ions(15a/15b) into said second layer of material (14') to modify a structure of the material of said second layer of material and thereby increase an etch selectivity of said second layer of material relative to said first layer of material (see figure 1e-1f, col. 11, lines 31-67, col. 12, lines 1-65), wherein the layer 14' has been removed). It is inherent that the implanted region would have a higher etch selectivity.

23. The method of claim 22, wherein said first layer of material comprises a gate electrode material (12, see col. 10, lines 33-34).

26. The method of claim 22, wherein said ions comprise at least one of argon

ions, xenon ions, germanium ions and silicon ions (see col. 11, lines 51-67).

27. The method of claim 22, wherein said ions are substantially inert ions (see col. 11, lines 51-67).

28. The method of claim 22, wherein an implant energy of an ion implant process performed to implant said ions is selected such that the structure of the material comprising the second layer of material is modified substantially throughout an entire thickness of said second layer of material (see figure 1e-1f).

30. The method of claim 22, further comprising performing at least one etch process to define a feature in said first layer of material (see figures 1a).

31. The method of claim30, further comprising performing an etching process to remove a portion of said second layer of material above said feature in said first layer of material (see figures 1b-1c, cols. 11, lines 7-30).

Referring to figures 1-10b, Long et al. teaches in claim 1, A method of forming a semiconductor device feature, the method comprising:

providing a substrate (204) having a first layer (212) formed thereon;

covering said substrate with a second layer of material (250);

implanting ions (see figure 6a-6b) into said second layer of material (250) to modify a structure of the material of said second layer (see figure 1D);

patterning said second layer of material (250) and said first layer by photolithography to form said semiconductor device feature in said first layer (see figure 7); and

removing said patterned second layer of material, whereby a selectivity in removing

said patterned second layer is increased by the implanting of said ions (see figure 9a-9b, col. 6, lines 54-67, col. 7, lines 1-18), wherein the layer 250 has been removed). It is inherent that the implanted region would have a higher etch selectivity, see col. 5, lines 44-65).

2. The method of claim 1, wherein said ions are substantially inert ions (see col. 5, lines 44-57).

3. The method of claim 1, wherein said ions are at least one of argon ions, xenon ions, germanium ions and silicon ions (see col. 5, lines 44-57).

7. The method of claim 1, wherein said layer of material is comprised of an inorganic material (250, oxide is an inorganic material).

22. A method, comprising:

providing a substrate (204) having a first layer of material (212) formed thereabove;

depositing a second layer of material (250) above said first layer of material; and implanting ions(see figure 6a-6b) into said second layer of material (250) to modify a structure of the material of said second layer of material and thereby increase an etch selectivity of said second layer of material relative to said first layer of material (see figure 9a-9b, col. 6, lines 54-67, col. 7, lines 1-18), wherein the layer 250 has been removed). It is inherent that the implanted region would have a higher etch selectivity, see col. 5, lines 44-65).

23. The method of claim 22, wherein said first layer of material comprises a gate electrode material (212, see col. 4, lines 29-34).

25. The method of claim 22, wherein said first layer of material comprises a gate electrode material and said second layer of material comprises an anti-reflective coating material.

26. The method of claim 22, wherein said ions comprise at least one of argon

ions, xenon ions, germanium ions and silicon ions (see col. 5, lines 44-57).

27. The method of claim 22, wherein said ions are substantially inert ions (see col. 5, lines 44-57).

28. The method of claim 22, wherein an implant energy of an ion implant process performed to implant said ions is selected such that the structure of the material comprising the second layer of material is modified substantially throughout an entire thickness of said second layer of material (see figure 6a-6b).

Regarding to claim 29, wherein an implant energy of an ion implant process performed to implant said ions is selected such that said implanted ions are substantially located adjacent an interface between said first layer of material and said second layer of material (see figures 6a-6b).

30. The method of claim 22, further comprising performing at least one etch process to define a feature in said first layer of material (see figures 4a-4b).

31. The method of claim 30, further comprising performing an etching process to remove a portion of said second layer of material above said feature in said first layer of material (see figures 6-8).

However, the reference does not teach the second layer is an antireflective layer a dimension of the device feature in one direction is 100 nm or less.

Iyer et al. teaches a silicon nitride or silicon oxide act as an antireflective layer (see abstract).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form a silicon nitride or silicon oxide to act as an

antireflective layer in process of Ishida et al. or Long et al. as taught by Iyer et al. because the process would prevent reflection of light so that the ion beam can go through.

It would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the dimension of the device feature, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.- dimension of the device feature in one direction is 100 nm or less), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- dimension of the device feature in one direction is 100 nm or less) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN